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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/971,054	10/05/2001	Toshimitsu Tamagawa	103213-00041	1215

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EXAMINER	
JERABEK, KELLY L	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/971,054	TAMAGAWA, TOSHIMITSU	
	Examiner	Art Unit	
	Kelly L. Jerabek	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6* is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 9/2/2005 have been fully considered but they are not persuasive.

Response to Remarks:

Applicant's arguments regarding claims 1-3 (Amendment pages 8-11) state that the combination of the Hosier and Perry references fails to teach or suggest that the metal conductor layer at the chip edge is formed integrally with and has the same width as the conductor layer surrounding the photoelectric conversion elements. The Examiner respectfully disagrees. Hosier discloses in figures 7-8 an interior and edge pixel layout of an image reading device consisting of a plurality of chips (10) mounted on a substrate (20). The device includes a plurality of photoelectric conversion elements (12) formed in rows on an IC chip (10) and a conductor layer (50) having openings for limiting light striking the photoelectric conversion elements (12) (col. 6, lines 12-65). **Hosier also discloses an opaque layer (100) that is formed integrally with the conductor layer (50) and in an area extending from a photoelectric conversion element (12) located at each end of the IC chip (10) to a chip edge (col. 6, lines 24-65).** However, although the Hosier reference discloses an opaque

layer (100) it fails to distinctly state that the opaque layer is a metal conductor layer having substantially a same width as the conductor layer (50).

Perry discloses in figure 2 a light sensitive IC including an opaque material deposited on the semiconductor substrate lateral edges. Perry states that the opaque material can be a variety of metals (such as aluminum, titanium, etc.) **and that the thickness of the opaque material layer will depend on the wavelength of light to be blocked (col. 5, lines 1-36).** Therefore, it would have been obvious for one skilled in the art to have been motivated to replace the opaque layer (100) disclosed by Hosier with a metal opaque layer as disclosed by Perry. Doing so would provide a means for blocking light (of the same wavelength as is blocked by conductor layer (50) at the edges of an IC (Perry: col. 5, lines 28-35). **The Examiner is reading the thickness of the metal opaque layer taught by Perry as the width of the metal opaque layer. Thus, it can be seen that the combination of the Hosier and Perry references teaches a conductor layer (50) (from Hosier) having openings and a metal opaque layer located at the chip edge (Perry) having a variable thickness depending on the wavelength of light to be blocked. The combination of the two references discloses two different opaque light blocking conductors that block light of the same frequency. Therefore, it can be seen that it is desirable to have the thickness of the two conductor layers (50) (from Hosier) and (metal opaque layer) (from Perry) be the same so that they block light of the same wavelength.**

Applicant's arguments regarding claims 1-3 (Amendment page 10) state that the combination of the Hosier and Perry references does not disclose a first metal conductor layer formed around the openings individually so as to prevent light from striking the photoelectric conversion elements except through the openings. The Examiner respectfully disagrees. Hosier discloses in figures 7-8 an interior and edge pixel layout of an image reading device consisting of a plurality of chips (10) mounted on a substrate (20). **The device includes a plurality of photoelectric conversion elements (12) formed in rows on an IC chip (10) and a conductor layer (50) having openings for limiting light striking the photoelectric conversion elements (12) (col. 6, lines 12-65). It can be seen in figures 7-8 that the metal conductor layer (50) is formed around openings individually so as to prevent light from striking the photoelectric conversion elements (12) except through the openings.** Hosier also discloses an opaque layer (100) that is formed integrally with the conductor layer (50) and in an area extending from a photoelectric conversion element (12) located at each end of the IC chip (10) to a chip edge (col. 6, lines 24-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 rejected under 35 U.S.C. 103(a) as being unpatentable over Hosier US 6,157,019 in view of Perry et al. US 6,548,323.

Hosier discloses in figures 7-8 an interior and edge pixel layout of an image reading device consisting of a plurality of chips (10) mounted on a substrate (20). **The device includes a plurality of photoelectric conversion elements (12) formed in rows on an IC chip (10) and a conductor layer (50) having openings for limiting light striking the photoelectric conversion elements (12) (col. 6, lines 12-65). It can be seen in figures 7-8 that the metal conductor layer (50) is formed around openings individually so as to prevent light from striking the photoelectric conversion elements (12) except through the openings.** Hosier also discloses an opaque layer (100) that is formed integrally with the conductor layer (50) and in an area extending from a photoelectric conversion element (12) located at each end of the IC chip (10) to a chip edge (col. 6, lines 24-65). However, although the Hosier reference discloses an opaque layer (100) it fails to distinctly state that the opaque layer is a metal conductor layer having substantially a same width as the conductor layer (50).

Perry discloses in figure 2 a light sensitive IC including an opaque material deposited on the semiconductor substrate lateral edges. Perry states that the opaque material can be a variety of metals (such as aluminum, titanium, etc.) and that the thickness of the opaque material layer will depend on the wavelength of light to be blocked (col. 5, lines 1-36). Therefore, it would have been obvious for one skilled in the

art to have been motivated to replace the opaque layer (100) disclosed by Hosier with a metal opaque layer as disclosed by Perry. Doing so would provide a means for blocking light (of the same wavelength as is blocked by conductor layer (50) at the edges of an IC (Perry: col. 5, lines 28-35). The Examiner is reading the thickness of the metal opaque layer taught by Perry as the width of the metal opaque layer. Thus, it can be seen that the combination of the Hosier and Perry references teaches a conductor layer (50) (from Hosier) having openings and a metal opaque layer located at the chip edge (Perry) having a variable thickness depending on the wavelength of light to be blocked. The combination of the two references discloses two different opaque light blocking conductors that block light of the same frequency. Therefore, it can be seen that it is desirable to have the thickness of the two conductor layers (50) (from Hosier) and (metal opaque layer) (from Perry) be the same so that they block light of the same wavelength.

Re claim 2, see claim 1.

Re claim 3, Hosier shows that the first conductor layer (50) and the opaque layer (100) are connected together by being formed continuously starting from the chip edge (figs. 7-8; col. 6, lines 12-65).

Allowable Subject Matter

Claim 7 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claim 7, the prior art does not teach or fairly suggest" An image reading device comprising an IC chip, the IC chip comprising: a plurality of photoelectric conversion elements...; a first metal conductor layer...; a second metal conductor layer having substantially the same width as the first metal conductor layer...; a semiconductor substrate..; an insulating layer; and a plurality of contact holes formed at predetermined intervals in at least one row in the insulating layer so as to surround each of the openings individually along every side thereof, the contact holes serving to connect the first metal conductor layer to the semiconductor substrate and simultaneously preventing light from striking the photoelectric conversion elements through openings other than particular openings".

Claim 6 is allowed.

The following is an examiner's statement of reasons for allowance:

Re claim 6, the prior art does not teach or fairly suggest" An image reading device comprising an IC chip, the IC chip comprising: a semiconductor substrate in which elements are formed; a plurality of photoelectric conversion elements...; an insulating layer...; a first metal conductor layer...; a second metal conductor layer having substantially the same width as the first metal conductor layer...; and a plurality of contact holes formed at predetermined intervals in at least one row in the insulating layer so as to surround each of the openings individually along every side thereof, the contact holes serving to connect the first metal conductor layer to the semiconductor substrate and simultaneously preventing light from striking the photoelectric conversion elements through openings rather than the openings formed right above the respective photoelectric conversion elements".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc Yen Vu can be reached on **(571) 272-7320**. The fax phone number for submitting all Official communications is 703-872-9306. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at **(571) 273-7312**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLJ

NGOC-YEN VU
PRIMARY EXAMINER